ABSTRACT OF THE DISCLOSURE

A test method provides a sample of wafer level defects most likely to cause yield loss on a semiconductor wafer subdivided into a plurality of integrated circuits (ICs). Defect size and location data from an inspection tool is manipulated in an algorithm based on defect sizes and geometry parameters. The defects are classified by defect size to form size based populations. The contribution of each size range of defect population to yield loss is calculated and random samples for review are selected from each defect size population. The number of samples from each size defect population is proportional to the predicted yield impact of each sample. The method is rapid and permits on-line process modification to reduce yield losses.